

## P-Channel 40 V (D-S) MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

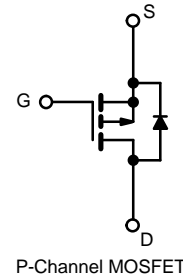
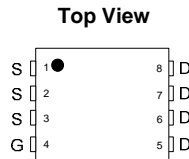
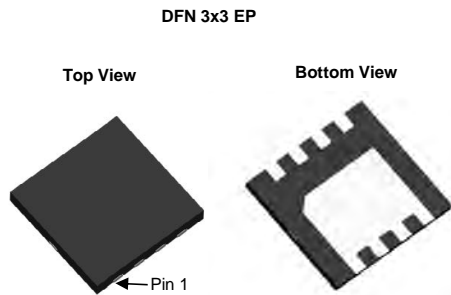
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 40	0.012 at V <sub>GS</sub> = - 10 V	- 45 <sup>d</sup>	43.1 nC
	0.013 at V <sub>GS</sub> = - 4.5 V	- 40 <sup>d</sup>	

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Low On-Resistance for Low Voltage Drop
- 100 % R<sub>g</sub> and UIS Tested

### APPLICATIONS

- Battery, Load and Adaptor Switches
  - Notebook Computers
  - Notebook Battery Packs



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 40	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20	V	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	- 45 <sup>d</sup>	A	
	T <sub>C</sub> = 70 °C	- 40 <sup>d</sup>		
	T <sub>A</sub> = 25 °C	- 33.1 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C	- 28.4 <sup>a, b</sup>		
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	- 100	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	- 50 <sup>d</sup>	A	
	T <sub>A</sub> = 25 °C	- 4.1 <sup>a, b</sup>		
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	- 25	
Single-Pulse Avalanche Energy		E <sub>AS</sub>	31.2	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	48	W
	T <sub>C</sub> = 70 °C		31	
	T <sub>A</sub> = 25 °C		5 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		3.2 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>			260	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	R <sub>thJA</sub>	21	25	°C/W
Maximum Junction-to-Case	Steady State	R <sub>thJC</sub>	2.1	2.6	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 70 °C/W.
- Package limited.
- The DFN3X3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

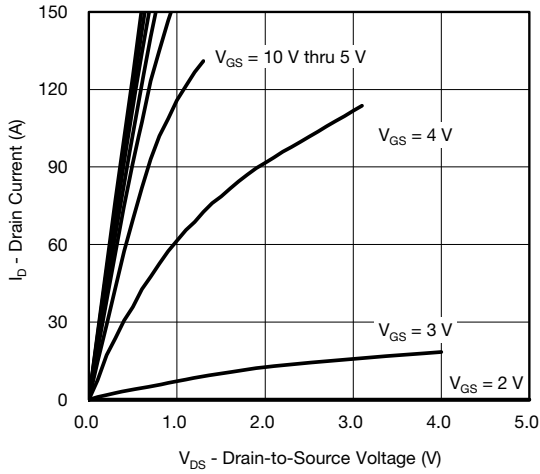
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = -250\text{ }\mu\text{A}$	-40			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-22		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.2		-2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	-30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -15\text{ A}$		0.012		$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		0.013		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -15\text{ A}$		60		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		5125		$\mu\text{F}$
Output Capacitance	$C_{oss}$			615		
Reverse Transfer Capacitance	$C_{rss}$			554		
Total Gate Charge	$Q_g$	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		90	135	nC
				43.1	65	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		13.6		nC
Gate-Drain Charge	$Q_{gd}$			28.8		
Gate Resistance	$R_g$		$f = 1\text{ MHz}$	0.5	2.4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		15	30	ns
Rise Time	$t_r$			12	24	
Turn-Off Delay Time	$t_{d(off)}$			58	110	
Fall Time	$t_f$			12	24	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		60	120	ns
Rise Time	$t_r$			60	120	
Turn-Off Delay Time	$t_{d(off)}$			52	100	
Fall Time	$t_f$			26	52	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-50	A
Pulse Diode Forward Current (100 $\mu\text{s}$ )	$I_{SM}$				-100	
Body Diode Voltage	$V_{SD}$	$I_S = -3\text{ A}, V_{GS} = 0$		-0.74	-1.20	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		23	46	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			12	24	nC
Reverse Recovery Fall Time	$t_a$			9		ns
Reverse Recovery Rise Time	$t_b$			14		

Notes:

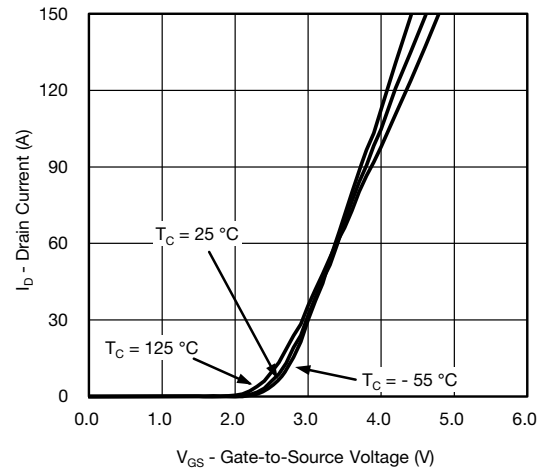
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

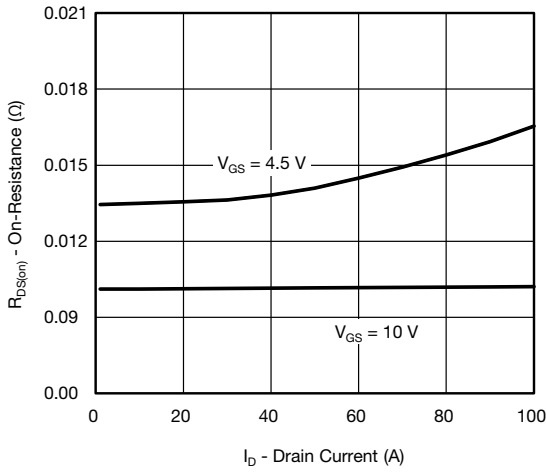
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



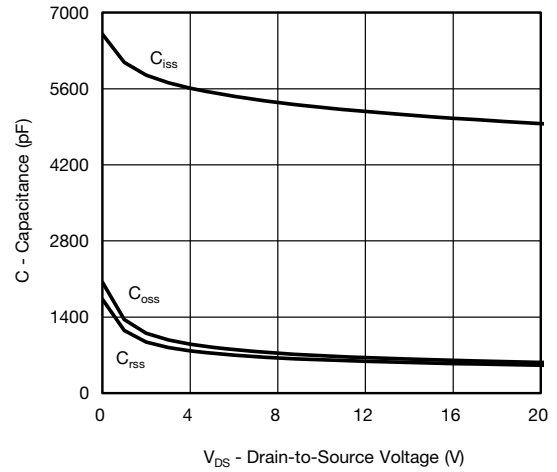
**Output Characteristics**



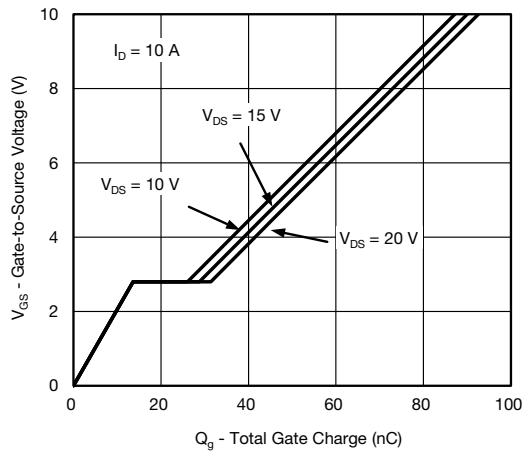
**Transfer Characteristics**



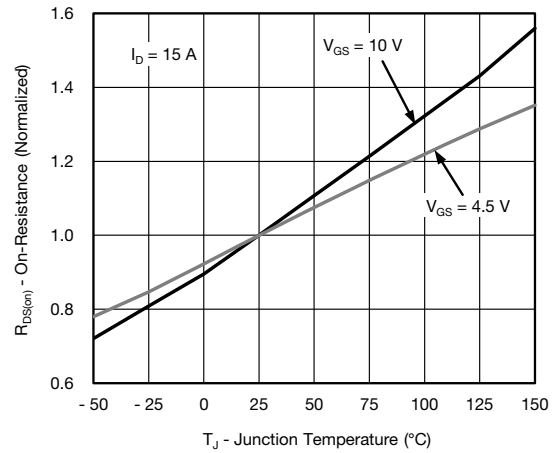
**On-Resistance vs. Drain Current**



**Capacitance**

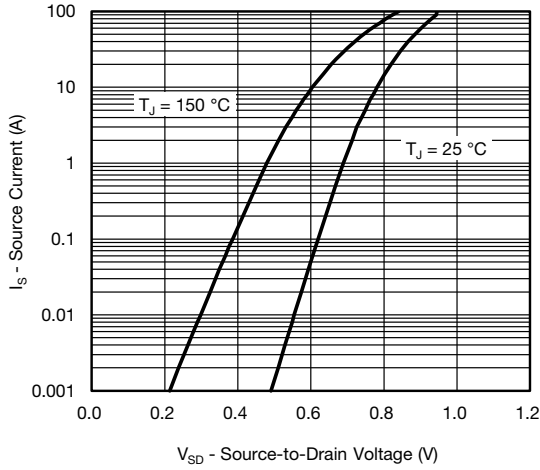


**Gate Charge**

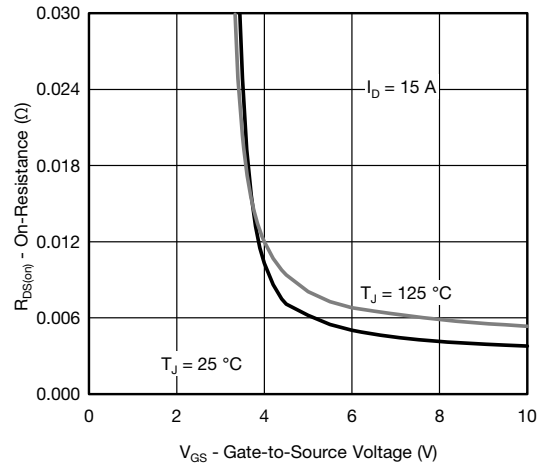


**On-Resistance vs. Junction Temperature**

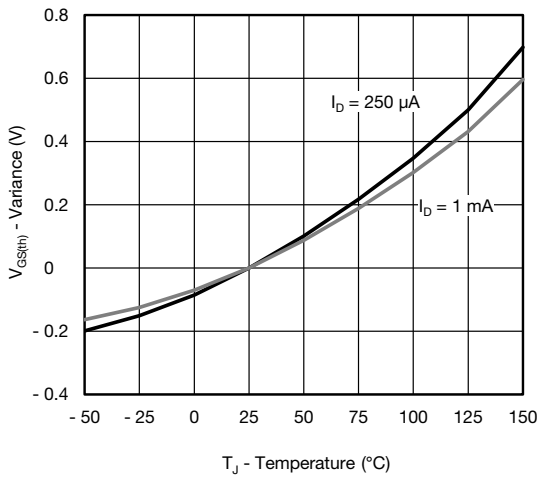
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



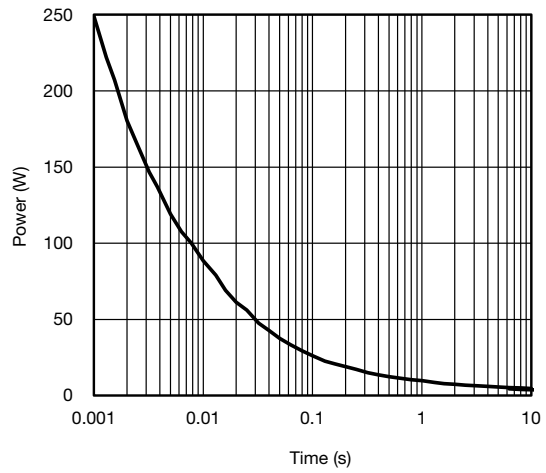
Source-Drain Diode Forward Voltage



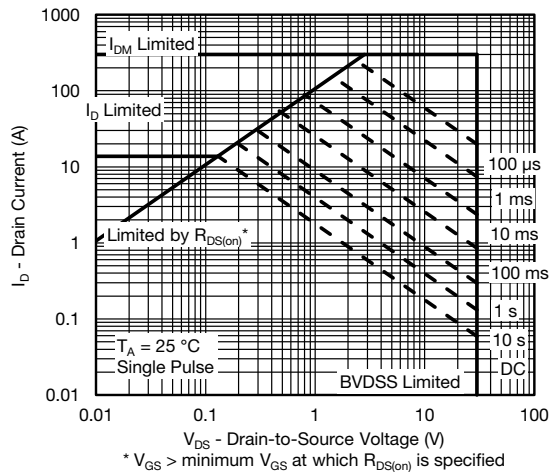
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

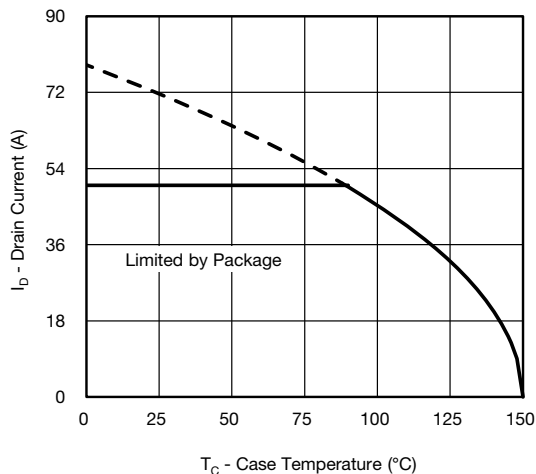


Single Pulse Power, Junction-to-Ambient

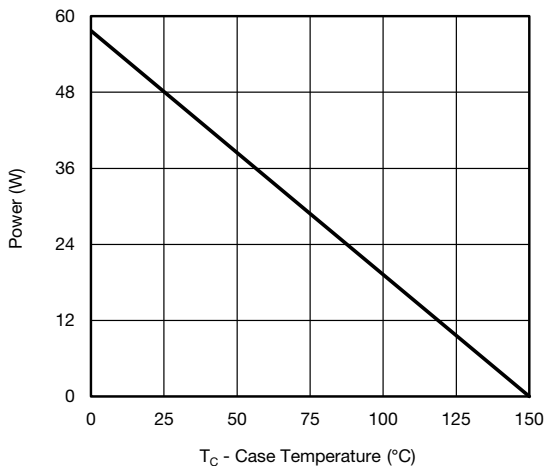


Safe Operating Area

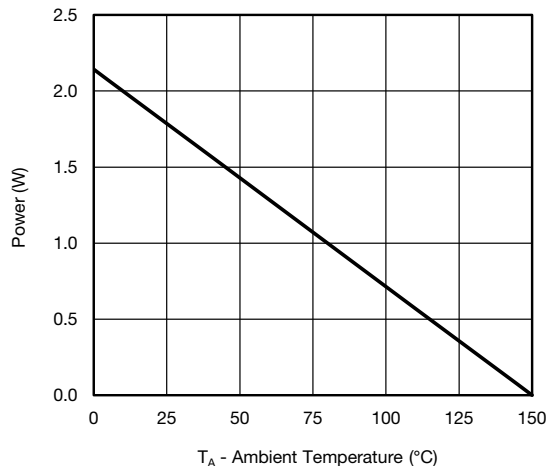
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



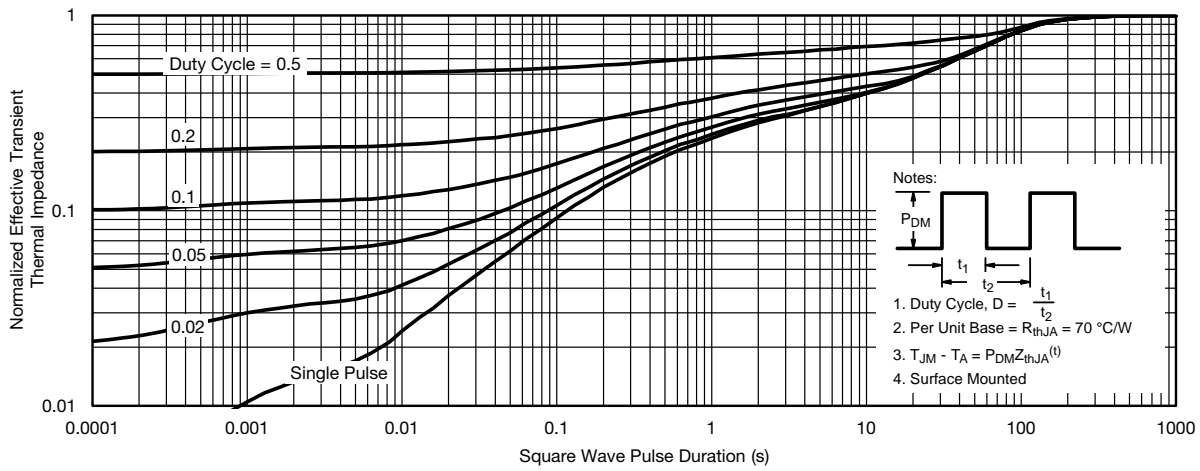
**Power, Junction-to-Case**



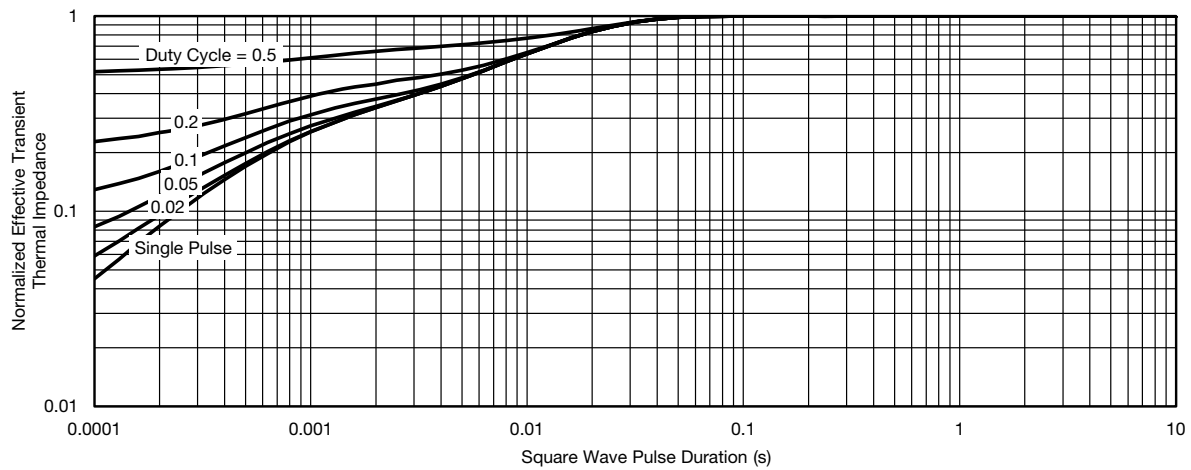
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

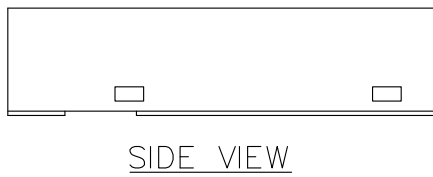
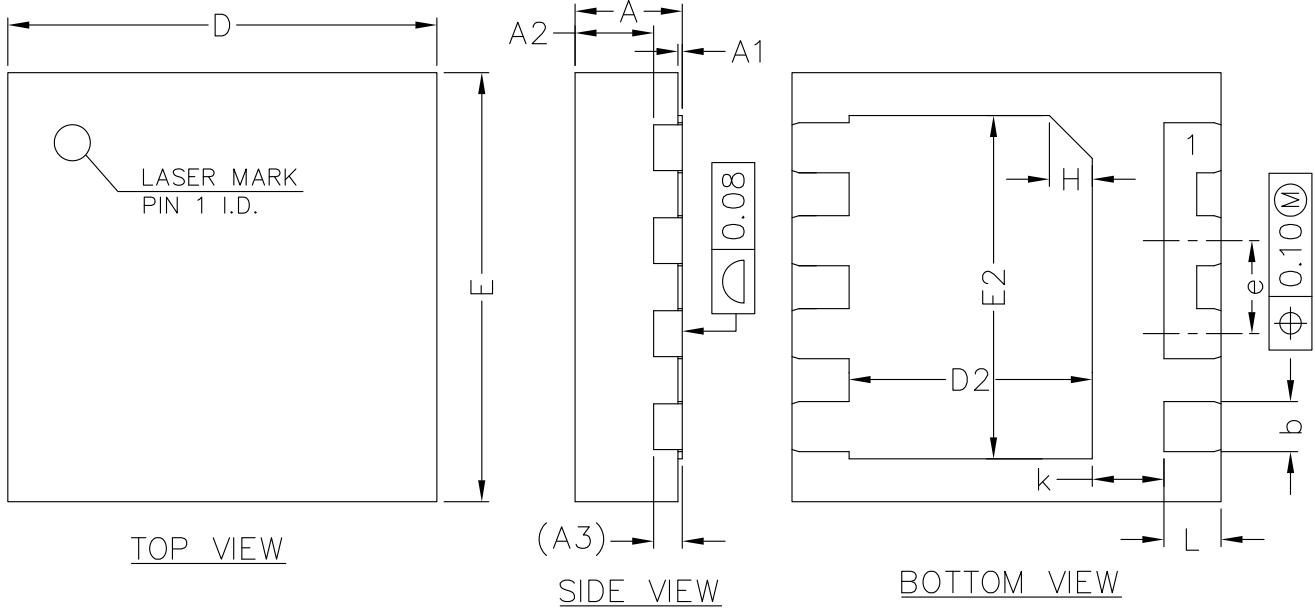
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.30	0.35	0.40
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.60	1.70	1.80
E2	2.30	2.40	2.50
e	0.55	0.65	0.75
K	0.40	0.50	0.60
L	0.35	0.40	0.45

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