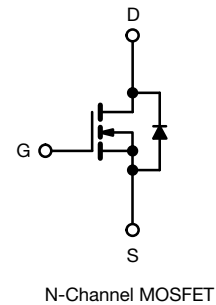


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	200	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.18
Q _g max. (nC)	70	
Q _{gs} (nC)	13	
Q _{gd} (nC)	39	
Configuration	Single	

FEATURES

- Surface mount
- Low-profile through-hole
- Available in tape and reel
- Dynamic dV/dt rating
- 150 °C operating temperature
- Fast switching
- Fully avalanche rated



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	200	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	I _D	T _C = 25 °C	18
			T _C = 100 °C	11
Pulsed Drain Current ^{a, e}		I _{DM}	72	A
Linear Derating Factor			1.0	
Single Pulse Avalanche Energy ^{b, e}		E _{AS}	580	mJ
Avalanche Current ^a		I _{AR}	18	A
Repetitive Avalanche Energy ^a		E _{AR}	13	mJ
Maximum Power Dissipation		P _D	T _C = 25 °C	130
			T _A = 25 °C	3.1
Peak Diode Recovery dV/dt ^{c, e}		dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) ^d		for 10 s	300	


Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 50 V, starting T_J = 25 °C, L = 2.7 mH, R_g = 25 Ω, I_{AS} = 18 A (see fig. 12).
- I_{SD} ≤ 18 A, dI/dt ≤ 150 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.
- Uses IRF640, SiHF640 data and test conditions.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^c	-	0.29	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V	-	-	25	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 125 °C	-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 11 A ^b	-	0.18	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 11 A ^d	6.7	-	-	S
Dynamic						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^d	-	1300	-	pF
Output Capacitance	C _{oss}		-	430	-	
Reverse Transfer Capacitance	C _{rss}		-	130	-	
Total Gate Charge	Q _g	V _{GS} = 10 V, I _D = 18 A, V _{DS} = 160 V, see fig. 6 and 13 ^{b, c}	-	-	70	nC
Gate-Source Charge	Q _{gs}		-	-	13	
Gate-Drain Charge	Q _{gd}		-	-	39	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 18 A, R _g = 9.1 Ω, R _D = 5.4 Ω, see fig. 10 ^{b, c}	-	14	-	ns
Rise Time	t _r		-	51	-	
Turn-Off Delay Time	t _{d(off)}		-	45	-	
Fall Time	t _f		-	36	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain	0.5	-	3.6	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	18	A
Pulsed Diode Forward Current ^a	I _{SM}		-	-	72	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 18 A, V _{GS} = 0 V ^b	-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 18 A, di/dt = 100 A/μs ^{b, c}	-	300	610	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	3.4	7.1	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. Uses IRF640/SiHF640 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

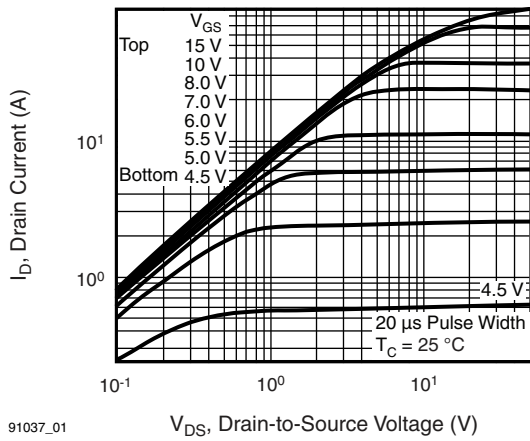


Fig. 1 - Typical Output Characteristics, T_J = 25 °C

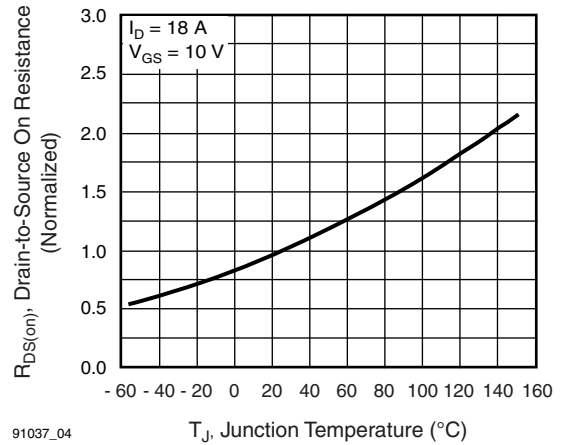


Fig. 4 - Normalized On-Resistance vs. Temperature

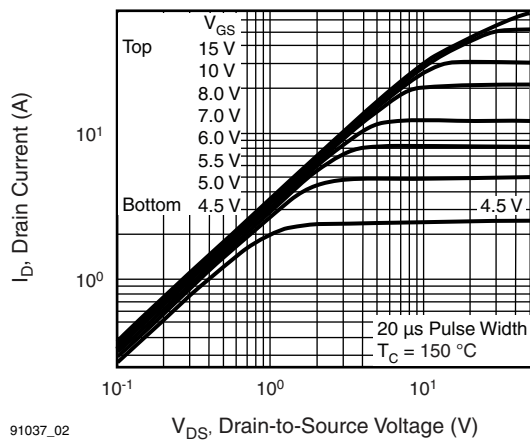


Fig. 2 - Typical Output Characteristics, T_J = 175 °C

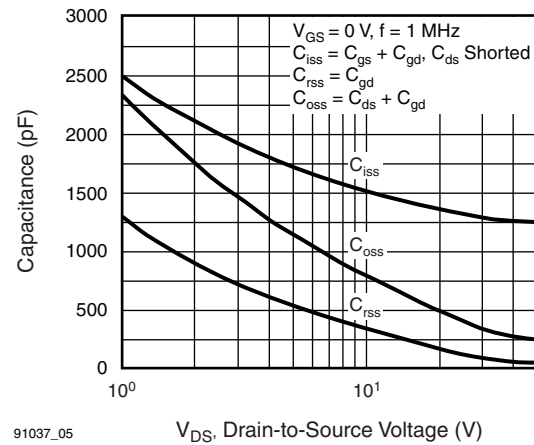


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

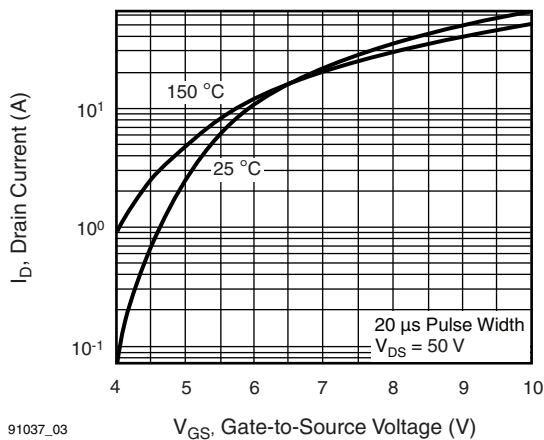


Fig. 3 - Typical Transfer Characteristics

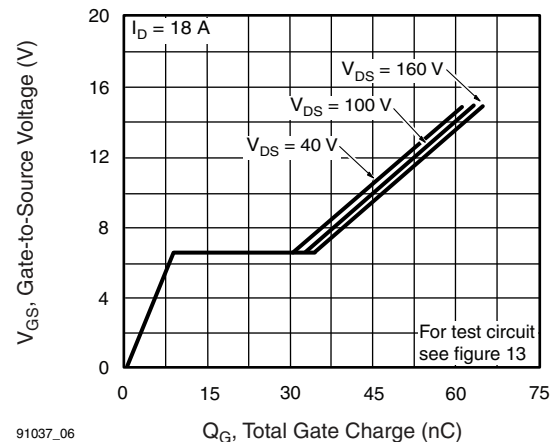
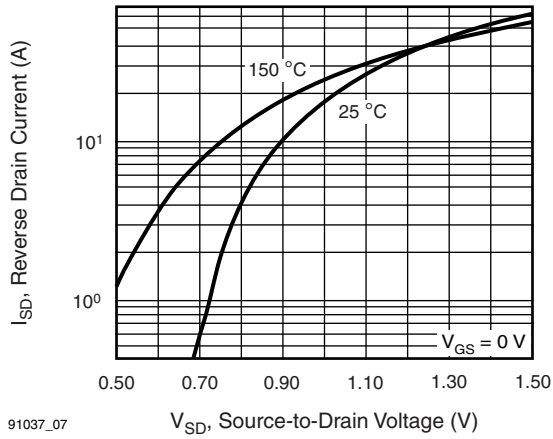
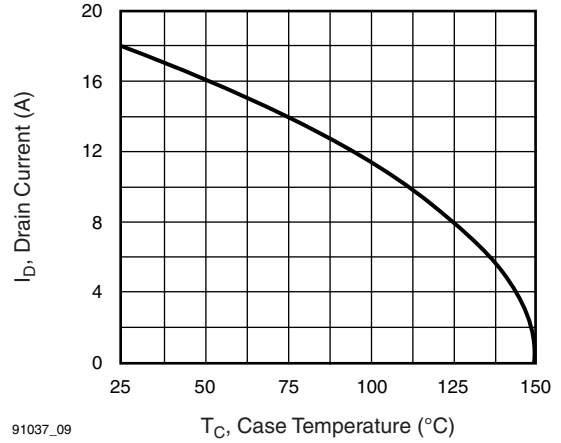


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



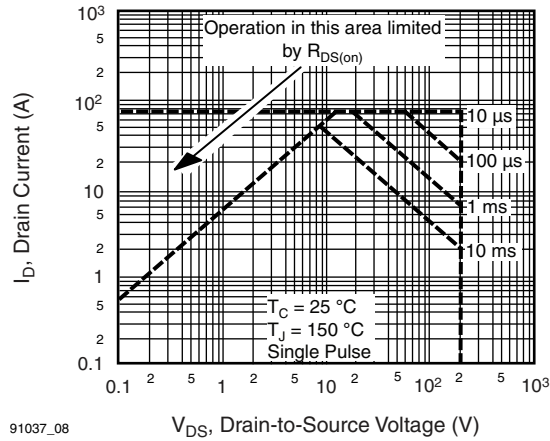
91037_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91037_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91037_08

Fig. 8 - Maximum Safe Operating Area

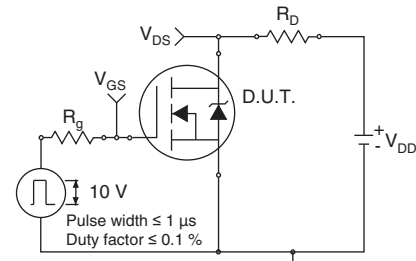


Fig. 10a - Switching Time Test Circuit

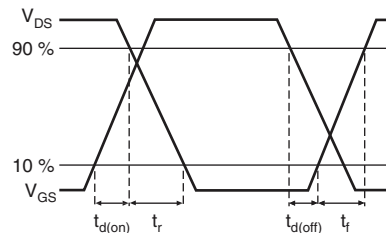
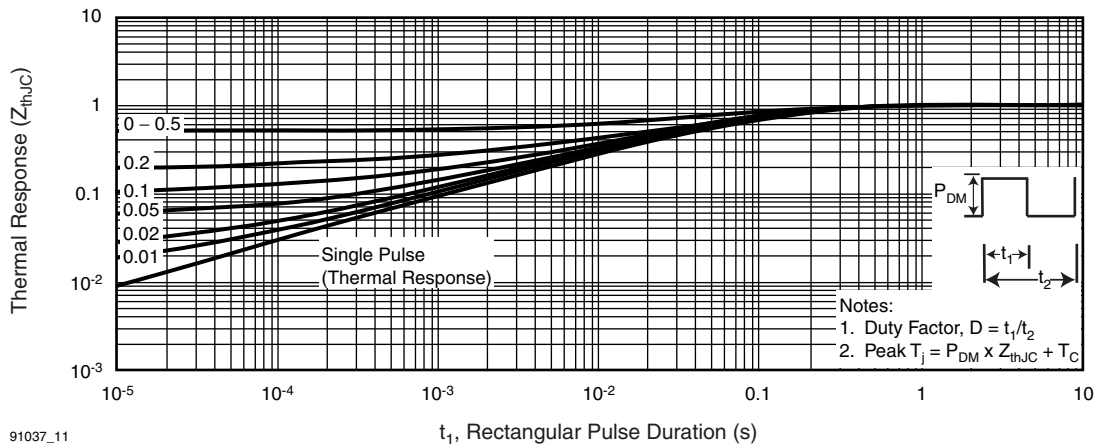


Fig. 10b - Switching Time Waveforms



91037_11

Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

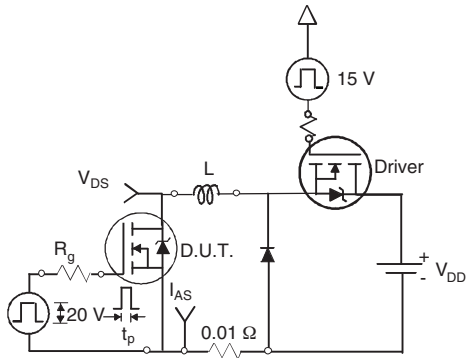


Fig. 12a - Unclamped Inductive Test Circuit

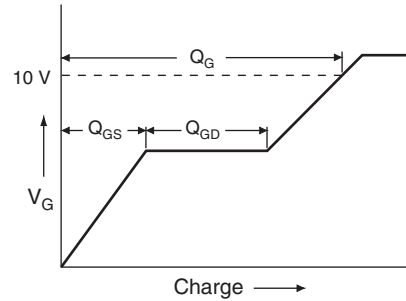


Fig. 13a - Basic Gate Charge Waveform

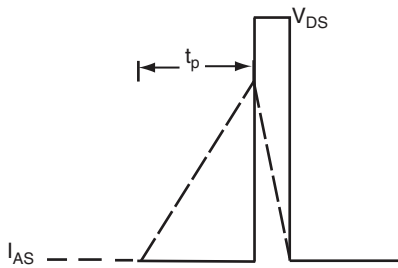


Fig. 12b - Unclamped Inductive Waveforms

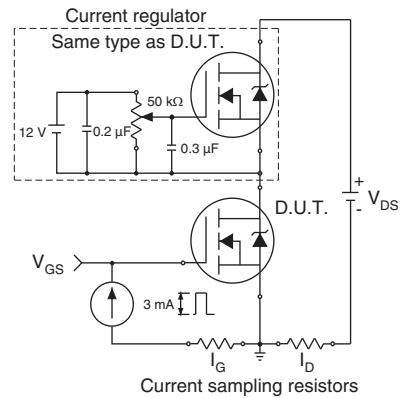


Fig. 13b - Gate Charge Test Circuit

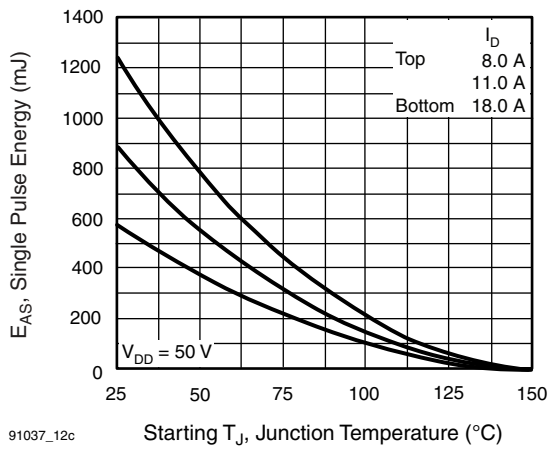
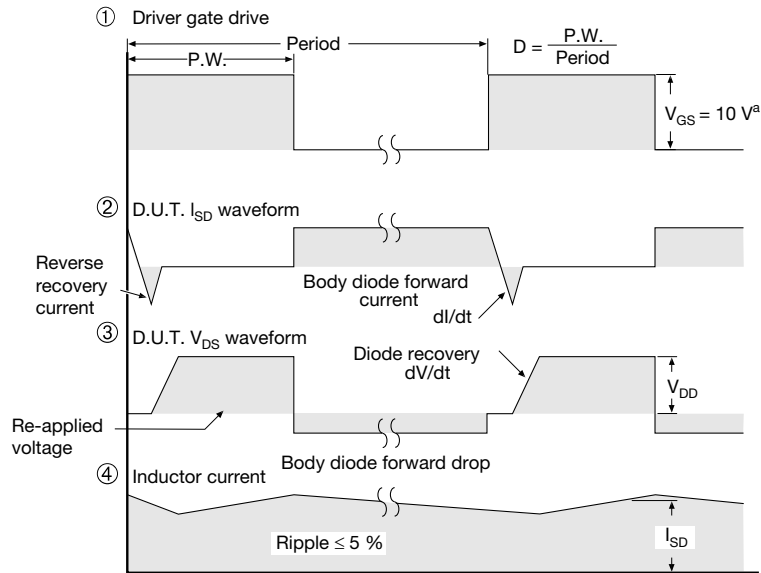
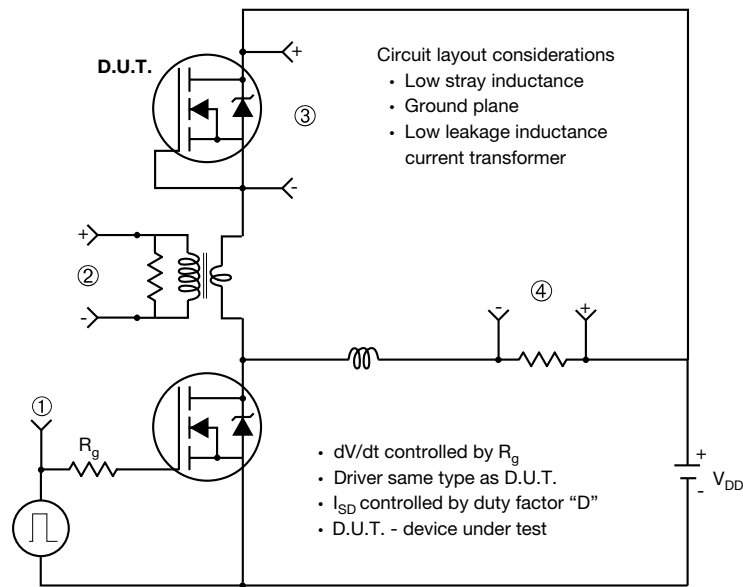


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

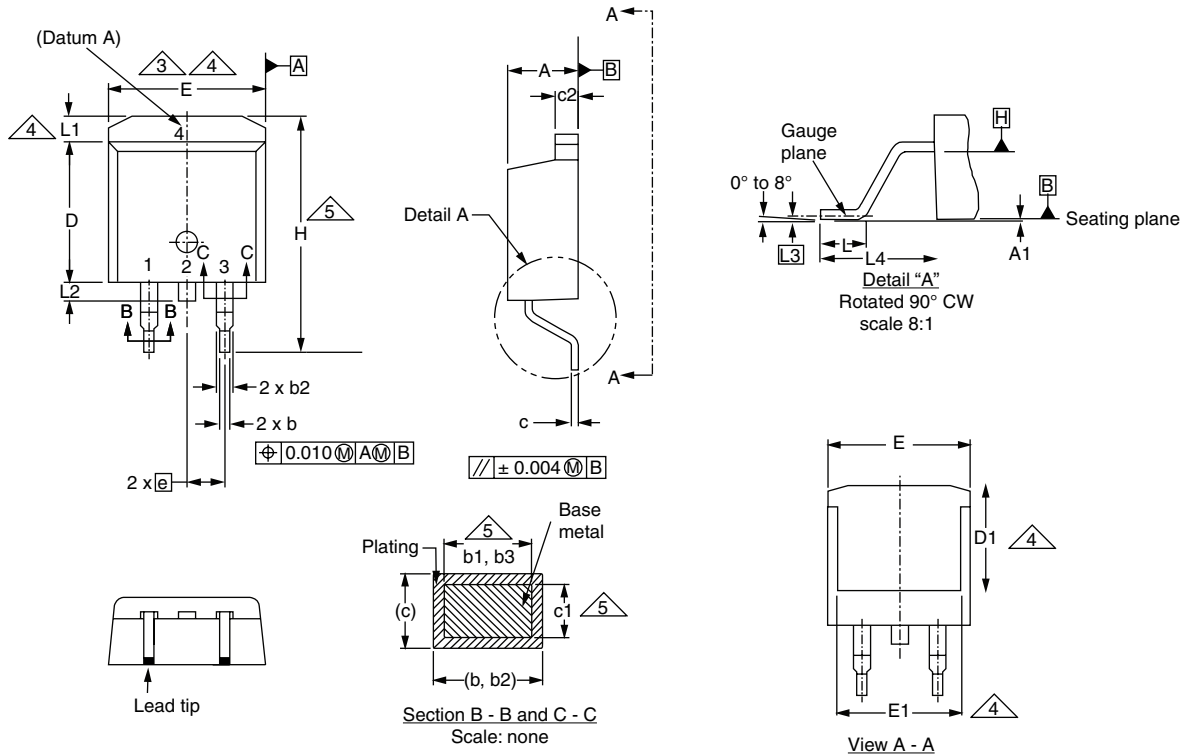
Peak Diode Recovery dV/dt Test Circuit



Note
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

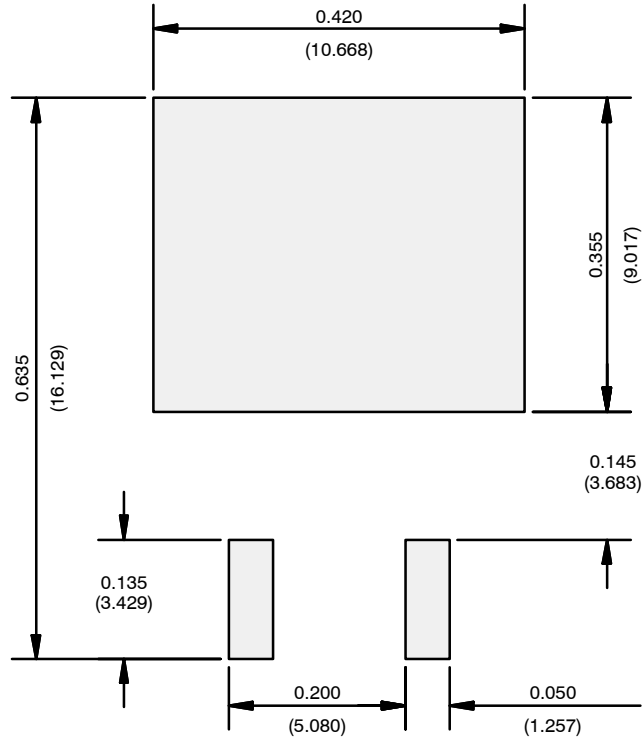
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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